Math. Appl. 15(2s)2026, 227–249

Fault-Tolerant Quantum Error Correction in Superconducting Qubit Arrays

Dharmesh Raju Rudraraju[1]

Abstract: *Useful quantum computation requires logical error rates many orders of magnitude below the error rates of physical qubits, and the surface code is the leading route to this goal for superconducting processors because it uses only nearest-neighbour interactions on a two-dimensional array. Whether a given device will actually benefit from encoding depends on a combination of gate fidelity, readout fidelity, decoherence during idle periods, and the speed of the classical decoder, and these parameters interact. This paper studies fault-tolerant error correction on superconducting arrays through circuit-level Monte Carlo simulation of the rotated surface code with minimum-weight perfect matching decoding. A uniform-noise sweep over distances 3 to 11 locates the error-suppression crossing at a physical error rate of about 1.0% to 1.1% for this noise model. Three device profiles built from gate error, readout error, and coherence time were then simulated: an early-generation profile (gate error 0.8%, readout error 3%, T1 = T2 = 20 μs) showed no suppression with distance ($\Lambda \approx 1.06$); a current-generation profile (0.3%, 0.8%, 70 μs) showed exponential suppression with $\Lambda \approx 2.7$, a logical error per round of 6.2×10^{-4} at distance 7; and a near-term target profile (0.2%, 0.5%, 120 μs) achieved $\Lambda \approx 4.3$. Extrapolating, a per-round logical error of 10^{-9} would need distance 35 (2,449 physical qubits per logical qubit) on the current profile and distance 23 (1,057 qubits) on the target profile. An error-budget analysis showed that gate error dominates: removing it reduced the logical error at distance 5 by about 90%, compared with 67% for idling error and 38% for readout error. A software matching decoder required about 1.0 μs per round at distance 9 on one CPU core, comparable to the cycle time, which indicates that real-time decoding is a first-order design constraint. The simulation omits leakage, crosstalk, and correlated bursts, and the paper discusses what those omissions imply, together with security considerations for the classical control stack.*

Introduction

Quantum computers promise advantages for chemistry, materials, optimisation, and cryptanalysis, but the algorithms that deliver these advantages need billions or trillions of operations, whereas the best physical qubits fail once in every hundred to thousand operations [17], [19]. Closing this gap requires quantum error correction, in which logical qubits are encoded redundantly across many physical qubits and errors are detected by repeatedly measuring parity checks without measuring the encoded information [1]–[3]. The threshold theorem guarantees that if physical error rates are below a constant threshold and noise has suitable structure, arbitrarily long computation is possible with polylogarithmic overhead [9]–[11]. In practice, the threshold is a property of a specific code, noise model, and decoder, and the overhead depends on how far below threshold a device operates.

[1]1424 Bliss Ave, Apt 1320, Allen, TX 75013

Keywords: Quantum Error Correction, Fault Tolerance, Surface Code, Superconducting Qubits, Transmon, Minimum-Weight Perfect Matching, Error Threshold, Real-Time Decoding.

Superconducting circuits are among the most advanced platforms for this task. Transmon qubits [18] are fabricated lithographically, interact through tunable couplers on a planar lattice, and execute gate and measurement cycles in about a microsecond [16], [17]. The surface code [4]–[7] matches this connectivity: each data qubit interacts only with four neighbouring measurement qubits, its threshold under circuit-level noise is on the order of one percent, and logical operations can be performed through lattice surgery [8], [35]. Recent experiments have moved from demonstrating small codes [14], [15] through first signs of error suppression [12] to exponential suppression of logical errors as the code distance increased from three to seven [13].

These advances raise an engineering question that this paper addresses: given a set of physical parameters, what will error correction deliver, and which parameter should be improved first? The answer depends on the interplay among gate error, readout error, idling decoherence, code distance, decoding speed, and the part of the noise that simple models omit. Quantitative simulation is the standard tool for answering such questions before devices exist, and modern stabiliser simulators and matching decoders make it possible to sample hundreds of thousands of error-correction shots in minutes [20], [21].

Following the Quality-by-Design approach of the reference study, which starts from a target profile, systematically ranks risks, and verifies results against pre-declared criteria, the paper makes four contributions.

1. A circuit-level simulation study of the rotated surface code under uniform noise that locates the error-suppression crossing for a standard noise model and reports the dependence of the logical error per round on distance.
2. A parameterised mapping from superconducting device characteristics (gate error, readout error, T1, T2) to circuit noise, used to simulate three device profiles and to extract the error-suppression factor Λ and the resource cost of projected logical error targets.
3. An error-budget sensitivity analysis that ranks the physical error sources by their influence on the logical error rate.
4. A measurement of software decoder throughput against the error-correction cycle time, together with a structured discussion of unmodelled error mechanisms and of security considerations for the classical control stack.

The remainder of the paper is organised as follows. Section II reviews the literature, Section III discusses related work, Section IV presents the methodology, Section V describes the experimental setup, Section VI reports results, Section VII discusses implications and limitations, and Section VIII concludes. All quantitative results are from simulation under the stated noise models and should not be read as measurements of any specific device.

LITERATURE REVIEW

A. Quantum error correction and stabiliser codes

Quantum information cannot be copied, and measurement disturbs it, so early doubts held that error correction was impossible. Shor [1] and Steane

[2] showed that redundancy can nevertheless protect a qubit against arbitrary single-qubit errors by encoding in entangled states and extracting an error syndrome that reveals the error without revealing the data. The stabiliser formalism of Gottesman [3] provided a compact description in which a code is defined by a group of commuting Pauli operators, the stabilisers, whose measured eigenvalues form the syndrome. A code that encodes k logical qubits in n physical qubits with distance d is denoted [[n, k, d]], and it can correct up to (d−1)/2 arbitrary errors.

B. Fault tolerance and the threshold theorem

Ordinary error correction assumes that the correction circuit itself is perfect. In practice, syndrome extraction involves faulty gates and measurements that can spread errors. Fault-tolerant protocols are designed so that a single fault produces at most a correctable error [11]. The threshold theorem establishes that for noise below a critical rate, concatenated codes allow arbitrarily accurate computation with modest overhead [9], [10]. Surface-code thresholds are calculated by numerical simulation, with code-capacity analyses mapping the problem to statistical-mechanical models and giving thresholds near ten percent for ideal syndrome measurement [5], and circuit-level analyses giving values of order one percent [6], [25]. The latter number is the one that matters for hardware, because it includes the noise of the syndrome-extraction circuit.

C. The surface code and lattice surgery

The surface code descends from Kitaev's toric code [4] and its planar variants with boundaries [7]. In the rotated layout used here, d^2 data qubits and d^2-1 measurement qubits are arranged on a square lattice, so that a logical qubit of distance d requires $2d^2-1$ physical qubits. X-type and Z-type parity checks of weight four, and weight two at the boundaries, are measured every cycle, and the pattern of changes in syndrome across cycles, the detection events, is passed to a decoder. Fault-tolerant logic operations between logical qubits can be implemented by lattice surgery, which merges and splits code patches and requires only local operations on the planar array [8], and compilation frameworks have shown how to organise large computations around such operations [35].

D. Superconducting hardware and its noise

Superconducting transmon qubits are anharmonic oscillators built from Josephson junctions [18]. Reviews describe their coherence limits, gate implementations, and readout [16], [17]. The main physical error sources are energy relaxation (T1) and dephasing (T2) during idle periods and gates, imperfect control pulses in single- and two-qubit gates, readout errors that arise from limited signal-to-noise and from qubit decay during measurement, and crosstalk between neighbouring elements. Superconducting devices also have error mechanisms that do not fit the standard Pauli models: population can leak out of the computational subspace to higher transmon levels, creating correlated errors that persist for many cycles unless removed by dedicated reset operations [27], [28], and ionising radiation such as cosmic rays can create bursts of correlated errors across large regions of a chip [29]. These mechanisms are not removed by increasing the code distance in the simple way that independent errors are, which is why they are central to the experimental

agenda.

E. Decoding

A decoder infers the most likely error from the detection events. For the surface code, minimum-weight perfect matching (MWPM) pairs detection events so that the total weight of the connecting error chains is minimal, a problem solved by Edmonds' blossom algorithm [22] and applied to topological codes since the earliest analyses [5]. Fowler showed that matching can be done in average constant parallel time per round [26], and recent implementations achieve around a million errors corrected per core-second [21]. Union-find decoders trade a small loss in accuracy for almost-linear time [23]. Because the quantum computation must wait for decoder output before applying certain logical operations, a decoder slower than the syndrome rate produces an exponentially growing backlog [24]. Proposed remedies include parallel window decoding [34] and dedicated hardware decoders [33].

F. Experimental demonstrations

Small repeated error-correction experiments with distance-three surface codes on 17 superconducting qubits were reported in 2022 [14], [15]. A 2023 experiment found that a distance-five logical qubit performed slightly better than a distance-three one, the first indication of suppression with scale [12]. A 2025 experiment on a 105-qubit processor reported error suppression by a factor of about 2.1 for each increase of two in distance up to distance seven, a logical error of roughly 0.14% per cycle at the largest distance, a cycle time of about a microsecond, and real-time decoding at distance five [13]. Alternative codes such as bivariate bicycle codes promise substantially lower overhead but require long-range connectivity [36]. These results motivate quantitative models that connect device parameters to logical performance.

RELATED WORK

Fowler et al. [6] provided the foundational circuit-level analysis of the surface code for large-scale quantum computing, with threshold estimates, overhead analysis, and a hardware-oriented description of the layout. Their analysis used a different noise model from the one here, so threshold values must be compared with care. Later resource estimation studies quantify the cost of useful algorithms: Gidney and Ekerå [30] estimated that factoring 2048-bit RSA integers would take about eight hours with 20 million noisy qubits under assumptions of a 0.1% physical error rate and a one-microsecond cycle time, and a 2025 update reduced the estimate to fewer than one million noisy qubits at the cost of a longer runtime [31]. Litinski [35] showed how to organise a computation as lattice surgery operations to minimise space and time overhead.

On the software side, Stim [20] provides fast sampling of stabiliser circuits with noise and automatic construction of detector error models, and PyMatching with sparse blossom [21] provides a fast MWPM decoder. These tools make it possible to explore parameter space at circuit level, which this paper does. The experimental papers [12]–[15] report measured logical error rates and suppression factors for specific devices, but they do not provide the sensitivity of the logical error to each physical parameter,

which can be obtained only by varying parameters independently in simulation. Table I summarises the positioning of this study.

TABLE I. Positioning of the Present Study Relative to Prior Work

Capability	Surface code theory [5], [6]	Resource estimation [30], [31], [35]	Experiments [12]–[15]	Present study
Circuit-level logical error vs distance	Yes	Assumed	Measured (device)	Simulated
Device-parameter to noise mapping	Partial	Assumed	Implicit	Explicit
Per-source error budget	No	No	Limited	Yes
Decoder throughput vs cycle time	No	No	Partial	Yes (software)
Leakage and burst errors	No	No	Yes	Not modelled

METHODOLOGY

A. Error-Correction Target Profile

The reference study began with a Quality Target Product Profile and derived Critical Quality Attributes. The same discipline is applied to error correction. The target profile for a superconducting error-correcting memory is (i) a simulated error-suppression crossing in the range of 0.5% to 1.5% for a standard circuit-level noise model, which tests that the simulation is consistent with published surface-code thresholds [6], [25]; (ii) exponential suppression with Λ of at least 2 for a current-generation device profile and at least 3 for a near-term target profile; (iii) a logical error per round below 10^{-3} at distance 7 on the current-generation profile; and (iv) a software decoding time per round no greater than the cycle time of 1 μs at distance 9. A fifth, qualitative requirement is that the dominant physical error source be identified so that engineering effort can be directed. The numerical thresholds are design targets for this study, not industry standards.

B. Code and Circuit

The rotated surface code with distance d encodes one logical qubit in d^2 data qubits, with d^2-1 measurement qubits that perform parity checks, using the parameters $[[d^2, 1, d]]$ and a physical qubit count of

$$n_{phys} = 2d^2 - 1 \qquad (1)$$

A logical qubit is stored as a quantum memory in the Z basis for r = d rounds of syndrome extraction followed by a final transversal measurement. Each round consists of resetting the measurement qubits, applying Hadamard gates, four layers of controlled-NOT gates between measurement and data qubits, further Hadamard gates, and measurement.

Circuits were generated by the Stim library [20]. The logical error is declared when the decoded correction disagrees with the actual change in the logical observable.

C. Noise Model and Device Profiles
Circuit-level noise was injected at four types of location, with the following parameters. A gate error rate pg applies depolarising noise after every one- and two-qubit gate. A readout error pm flips each measurement outcome. A reset error equal to pg flips each reset. A data-qubit idle error pi applies single-qubit depolarising noise to every data qubit once per round, representing decoherence while measurement qubits are being measured and reset. Rather than choosing pi arbitrarily, it is derived from the coherence times through the Pauli-twirled amplitude and phase damping channel over an idle duration t:

$$p_x = p_y = (1 - e^{-t/T1}) / 4, \quad p_z = (1 - e^{-t/T2}) / 2 - p_x, \quad p_i = p_x + p_y + p_z \qquad (2)$$

with t = 0.6 μs of exposure in a cycle of 1.0 μs, since data qubits are not idle for the entire cycle. Table II lists the three device profiles. They were chosen to span the range from early devices to near-term targets and are representative rather than descriptions of specific processors.

TABLE II. Device Profiles and Derived Circuit-Noise Parameters

Profile	Gate error p_g	Readout error p_m	T1 = T2 (μs)	Idle error p_i	Role
A Early-generation	0.8%	3.0%	20	2.22%	Above threshold
B Current-generation	0.3%	0.8%	70	0.64%	Realistic today
C Near-term target	0.2%	0.5%	120	0.37%	Improvement goal

D. Decoding
The detector error model of each circuit was extracted by Stim and converted to a matching graph in which detectors are nodes and error mechanisms are edges weighted by the log-likelihood ratio of the mechanism,

$$w_e = \ln((1 - p_e) / p_e) \qquad (3)$$

and decoding was performed by PyMatching [21], an implementation of MWPM using the sparse blossom algorithm. Decoding used the true noise parameters, which corresponds to a perfectly calibrated decoder. Real decoders must be calibrated from device data, and calibration errors are an additional source of performance loss that is not modelled.

E. Metrics
The probability PL that the logical observable is wrongly decoded after r rounds is converted into a per-round logical error by assuming independent, identically distributed rounds:

$$\varepsilon = ½ [1 - (1 - 2 P_L)^{1/r}] \quad (4)$$

The statistical uncertainty of each estimate is binomial,

$$\sigma_P = \sqrt{(P_L (1 - P_L) / N)} \qquad (5)$$

where N is the number of shots. Below threshold, the logical error per round is expected to decrease exponentially with the distance,

$$\varepsilon d = C \Lambda^{-(d+1)/2}, \quad \Lambda = \varepsilon d / \varepsilon d+2 \qquad (6)$$

where Λ is the error-suppression factor, which is approximately the ratio of the threshold to the physical error rate [12], [13]. For each profile, C and Λ were estimated by least-squares regression of ln ε on (d+1)/2 using distances 3 to 9, and the distance needed for a target logical error ε* was extrapolated as

$$d^* = 2 \ln(C / \varepsilon^*) / \ln \Lambda - 1, \quad \text{rounded up to an odd integer} \qquad (7)$$

The projection assumes that exponential suppression continues, which is an optimistic assumption because unmodelled correlated errors can limit it, and the results are labelled as such. The decoder timing metric is the average wall-clock decoding time per round per shot in batch mode on a single CPU core. The condition for the decoder not to accumulate a backlog is that the decoding time per round does not exceed the syndrome-generation time,

$$R = t_{dec} / t_{cycle} \leq 1 \qquad (8)$$

since if R exceeds one the queue of undecoded syndromes grows exponentially with the depth of the computation [24].

F. Risk Assessment

Risks to the performance of a fault-tolerant memory were ranked with a Failure Mode and Effects Analysis style risk priority number,

$$RPN = S \times O \times D \qquad (9)$$

with S the severity, O the occurrence likelihood, and D the difficulty of detection, each scored from 1 to 10. The scores in Table III are the authors' judgements and serve as a worked example of the procedure. Threats with an RPN of at least 250 were treated as priorities, and Table III indicates which threats are addressed by the simulations in this paper.

TABLE III. Risk Assessment of Threats to Fault-Tolerant Operation

Threat	S	O	D	RPN	Addressed here
Leakage and leakage-induced correlated errors	8	6	7	336	No (not modelled)
Decoder latency and syndrome backlog	8	6	7	336	Yes (timing)
Calibration drift and readout instability	7	7	6	294	Partly (sensitivity)
Crosstalk between neighbouring qubits	7	6	6	252	No (not modelled)
Two-qubit gate error	9	8	3	216	Yes
Control-stack integrity (tampering with decoder or calibration data)	9	3	7	189	Discussed
Idle decoherence and defects in two-level systems	6	6	5	180	Yes
Cosmic-ray and other burst errors	9	3	6	162	No (not modelled)

EXPERIMENTAL SETUP

A. Software and Environment

Circuits were generated and sampled with Stim [20], and decoded with PyMatching [21]. Experiments ran on a single general-purpose CPU workstation in Python. The generated circuits implement the standard rotated surface-code memory experiment, and the noise parameters were supplied as described in Section IV. The scripts are provided as supplementary material so that every number can be regenerated.

B. Uniform-Noise Threshold Sweep

All four noise parameters were set equal to a single physical error rate p, which was varied from 0.3% to 1.2% in ten steps. Distances 3, 5, 7, 9, and 11 were simulated, each with d rounds. Shots per point were 300,000 for distances 3 to 7, 200,000 for distance 9, and 100,000 for distance 11. The crossing point was estimated for pairs of distances by log-linear interpolation of the per-round logical error.

C. Device-Profile Simulations

Each of the three profiles in Table II was simulated at distances 3, 5, 7, and 9, with d rounds. Shot counts were 30,000 to 50,000 for profile A, 300,000 to 400,000 for profile B, and 600,000 to 1,000,000 for profile C, chosen so that at least 100 logical errors were observed at every point. The smallest count was 129 errors (profile C, distance 9), which corresponds to a relative statistical uncertainty of about 9%.

D. Sensitivity Analysis and Decoder Timing

Starting from profile B at distance 5 with 400,000 shots per point, each of the three error sources, the gate error, the readout error, and the idle error, was scaled by 0, 0.5, 1, and 2 with the others held fixed. Decoder timing used uniform noise at p = 0.3%, distances from 3 to 21 with d rounds, and 5,000 shots decoded in one batch after a warm-up batch. Timing reflects throughput on a single core and not the latency of a streaming real-time decoder.

RESULTS

A. Error Suppression and Crossing Under Uniform Noise

Figure 2 and Table IV show the logical error per round under uniform noise. At low physical error rates, increasing the distance reduced the logical error strongly. At p = 0.5%, the logical error per round fell from 5.8×10^{-3} at distance 3 to 4.2×10^{-4} at distance 11, a factor of about 14, which corresponds to a suppression factor of about 1.9 for each increase of two in distance. At p = 0.3%, the reduction from distance 3 to 11 was more than a factor of 100. At high physical error rates the ordering reversed: at p = 1.2% the distance-11 code was worse than the distance-3 code (3.2×10^{-2} against 2.9×10^{-2}). The curves cross at the error-suppression crossing, and Table V gives its estimate for several pairs of distances.

TABLE IV. Logical Error per Round Under Uniform Noise (units of 10^{-3})

p	d = 3	d = 5	d = 7	d = 9	d = 11
0.3%	2.18	0.67	0.20	0.066	0.017
0.5%	5.81	2.84	1.48	0.75	0.42
0.7%	10.92	7.22	4.88	3.61	2.58
0.9%	16.73	13.87	11.54	10.29	9.51
1.1%	24.41	22.81	21.97	21.87	22.73

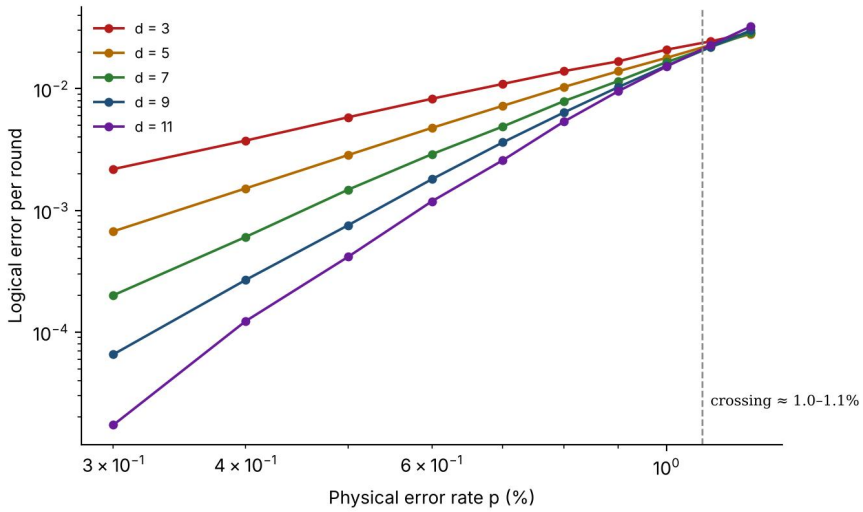

Figure 2: Logical error per round versus physical error rate for distances 3 to 11

The estimated crossing was 1.17% for distances 5 and 7, 1.11% for 7 and 9, and 1.03% for 9 and 11, with pairs spanning larger differences giving 1.14% (5 and 9) and 1.07% (7 and 11). The estimate drifted downward as larger codes were used, which is a known finite-size effect, and the asymptotic threshold for this noise model is therefore likely to be around 1.0% to 1.1%, inside the pre-declared range of 0.5% to 1.5%. This value is higher than the roughly 0.6% quoted for some other circuit-level noise models [6], because the noise model here places errors only at the locations listed in Section IV, with no noise on idle measurement qubits and a single depolarising channel after each gate. The number is therefore best read as a property of this model.

TABLE V. Estimated Error-Suppression Crossing by Pair of Distances

Distance pair	Crossing (p)	Comment
5 and 7	1.17%	Smallest codes
7 and 9	1.11%	
9 and 11	1.03%	Largest codes
5 and 9	1.14%	
7 and 11	1.07%	

B. Device Profiles and the Suppression Factor

Table VI gives the results for the three device profiles, and Figure 3 plots them. The early-generation profile showed no suppression: the logical error per round was 3.8×10^{-2} at distance 3 and 3.1×10^{-2} at distance 9, giving a fitted Λ of 1.06. The combination of a 0.8% gate error, a 3% readout error, and a 2.2% idle error places this device above the threshold of the circuit, and encoding in larger codes brings no benefit. The current-generation profile achieved clear exponential suppression, with successive ratios of 2.76, 2.61, and 2.68 and a fitted Λ of 2.68. The logical error per round fell from 4.5×10^{-3} at distance 3 to 2.3×10^{-4} at distance 9, and was 6.2×10^{-4} at distance 7, satisfying the criterion of being below 10^{-3}. The near-term target profile gave successive ratios of 4.36, 4.39, and 4.18 and a fitted Λ of 4.31, with a per-round logical error of 2.4×10^{-5} at distance 9. The result for profile B is somewhat above the suppression factor of about 2.1 reported for a recent experiment [13], which is consistent with the simulation omitting error mechanisms that exist in real hardware.

TABLE VI. Logical Error per Round by Device Profile and Distance (units of 10^{-3}), with Logical Errors Counted

Profile	d = 3	d = 5	d = 7	d = 9	Fitted Λ
A Early-generation	37.87 (5261)	32.31 (7099)	32.17 (9304)	31.46 (6643)	1.06
B Current-generation	4.49 (5343)	1.63 (3233)	0.62 (1739)	0.23 (626)	2.68
C Near-term target	1.91 (5704)	0.44 (2186)	0.100 (698)	0.024 (129)	4.31

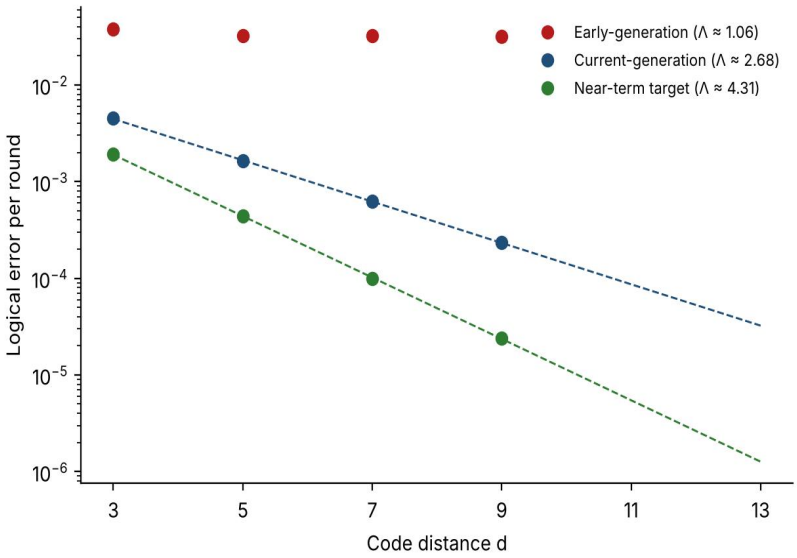

Figure 3: Logical error per round versus code distance for the three device profiles, with exponential fits (dashed)

C. Projected Resource Cost

Extrapolating the fits gives the distances and physical-qubit counts in Table VII. On the current-generation profile, a per-round logical error of 10^{-6} would need distance 21 and 881 physical qubits per logical qubit, 10^{-9} would need distance 35 and 2,449 qubits, and 10^{-12} would need distance 49 and 4,801 qubits. The near-term target profile reduces these to distances 15, 23, and 33 and to 449, 1,057, and 2,177 qubits. Improving Λ from 2.7 to 4.3, which required a 33% reduction in gate error, a 38% reduction in readout error, and a 70% increase in coherence time, therefore reduced the qubit overhead for a 10^{-9} target by a factor of about 2.3. Because the overhead depends on Λ through the logarithm in the distance formula, each increment in Λ gives diminishing but still substantial returns. These projections are optimistic, as they assume that independent errors remain the limiting mechanism at large distance, and they should be treated as lower bounds on the overhead.

TABLE VII. Projected Distance and Physical Qubits per Logical Qubit

Profile (fitted Λ)	Target per round	Distance d*	Qubits $2d^{*2} - 1$	Reduction vs B
B (2.68)	10^{-6}	21	881	–
C (4.31)	10^{-6}	15	449	2.0×
B (2.68)	10^{-9}	35	2,449	–
C (4.31)	10^{-9}	23	1,057	2.3×
B (2.68)	10^{-12}	49	4,801	–
C (4.31)	10^{-12}	33	2,177	2.2×

D. Error Budget

Table VIII reports the sensitivity analysis at distance 5 for profile B. Eliminating the gate error reduced the logical error per round by 90%, from 1.59×10^{-3} to 0.17×10^{-3}. Eliminating the idle error reduced it by 67%, and eliminating the readout error by only 38%. The dependence on the gate error was steeply nonlinear: halving it reduced the logical error by a factor of 2.4, and doubling it increased the logical error by a factor of 3.3, which corresponds to a local power-law exponent between 1.2 and 1.7, higher than the first power that would apply if errors acted independently. The reductions from eliminating individual sources add up to more than 100%, which shows that the sources interact: the logical error depends on combinations of faults, and the removal of one source lowers the probability of many combined events. The practical implication is that two-qubit gate fidelity is the first lever to pull on the current profile, followed by idle decoherence, with readout error the least influential of the three, although readout also determines the speed of the cycle, which is not captured here.

TABLE VIII. Logical Error per Round at Distance 5 When Scaling One Error Source (units of 10^{-3}; profile B)

Scaled source	× 0	× 0.5	× 1	× 2	Δ at × 0
Gate error p_g	0.17	0.67	1.59	5.22	−90%
Idle error p_i	0.53	1.01	1.60	3.47	−67%
Readout error p_m	1.01	1.31	1.63	2.54	−38%

E. Decoder Throughput

Table IX shows the software decoder timing. At p = 0.3%, decoding required 0.04 µs per round at distance 3, 0.23 µs at distance 5, 0.54 µs at distance 7, and 1.00 µs at distance 9, which equals the one-microsecond cycle time assumed for the device. At distance 15, the time was 3.4 µs per round, and at distance 21 it was 8.4 µs. Over distances 5 to 21 the time per round scaled roughly as the 2.5th power of the distance, faster than the quadratic growth in the number of syndrome bits per round, which is consistent with the increase in the number of detection events to be matched. A single core therefore keeps up with the syndrome stream only up to about distance 9 at this noise level, and larger codes, which are exactly the ones needed for algorithms, require parallel decoding or specialised hardware to avoid the exponential backlog described in Section IV. The measurement is of throughput in batch mode, and a streaming decoder also has latency requirements for operations that depend on decoding results, which were not measured.

TABLE IX. Software MWPM Decoding Time per Round (single core, p = 0.3%)

Distance d	Mean detection events per shot	Decoding time per round (μs)	Ratio R to 1 μs cycle
3	0.8	0.04	0.04
5	5.1	0.23	0.23
7	15.5	0.54	0.54
9	34.9	1.00	1.00
11	65.3	1.57	1.57
15	171.6	3.43	3.43
21	483.6	8.38	8.38

F. Verification Against the Target Profile

Table X compares the results with the target profile. Three of the four quantitative criteria were met, and the decoder criterion was met only marginally and not at the pre-declared value. The dominant error source was identified as the two-qubit gate error.

TABLE X. Verification Against the Error-Correction Target Profile

Criterion	Target	Result	Met
Crossing under uniform noise	0.5%–1.5%	1.0%–1.1% (drifting down with size)	Yes
Λ for profiles B and C	≥ 2 and ≥ 3	2.68 and 4.31	Yes
Logical error per round at d = 7, profile B	$< 10^{-3}$	6.2×10^{-4}	Yes
Decoding time per round at d = 9	≤ 1 μs	1.00 μs (1.0005)	Marginal
Dominant error source identified	Qualitative	Two-qubit gate error	Yes

DISCUSSION

The simulations support a simple picture of the economics of error correction on superconducting hardware. There is a sharp transition: on the early-generation profile, which sits above the circuit threshold, encoding made no difference, whereas on the current-generation profile, a combination of moderately better gate fidelity, readout, and coherence produced a suppression factor of 2.7 and put the device in the regime in which every increase in distance pays off. The overhead is then set by Λ, and the improvement from 2.7 to 4.3 cuts the cost of a 10^{-9} logical qubit by more than half. This is why experiments emphasise Λ as the central figure of merit and why the improvement of a few tenths of a percent in gate error is considered significant.

The error-budget analysis identifies where to invest. Two-qubit gate errors dominate because each stabiliser measurement involves four such gates and

because they can propagate errors from the measurement qubit to several data qubits. The analysis is a first-order guide: gate error in the simulation is a single depolarising channel, whereas real gates have error contributions from decoherence during the gate, control imperfections, and coupling to spectator qubits, each with its own remedy. The finding that readout error is the least influential of the three should also be treated with care, because faster or higher-fidelity readout also shortens the cycle, which reduces idle error through a mechanism that the sensitivity analysis holds fixed.

The decoder results illustrate a point that is sometimes overlooked in device-oriented discussions. A software decoder on one core already approaches the cycle time at distance 9, and the cost grows faster than the number of qubits. Large logical qubits and thousands of them are impossible without decoders that run in parallel, for example by decomposing the problem in time into overlapping windows [34], or in dedicated hardware that sits close to the cryogenic control electronics [33]. The error-correction problem is therefore a joint quantum–classical systems problem.

What the simulation does not capture

Three classes of error mechanisms that matter in superconducting devices are absent from the model. Leakage of population out of the computational subspace creates errors that are correlated in space and time and that standard decoders do not handle, and experiments therefore include leakage removal operations [27], [28]. Crosstalk and frequency collisions create correlated errors between neighbouring qubits that violate the independence assumption behind the exponential-suppression formula. Rare bursts of correlated errors from ionising radiation can affect many qubits simultaneously and are not suppressed by increasing the distance unless the hardware is shielded or engineered against them [29]. In addition, the model uses a perfectly calibrated decoder, a uniform noise level across qubits, and a Pauli noise approximation to amplitude damping. Real processors have a broad distribution of qubit and gate quality, and the performance of a code is often dominated by its worst components. These omissions explain why the simulated Λ of 2.7 for a profile resembling today's devices exceeds the roughly 2.1 observed in experiments [13], and they imply that the resource projections in this paper are lower bounds.

Security considerations for the control stack

A fault-tolerant quantum computer is also a distributed classical system, and its classical layers have security properties that deserve explicit attention. Two aspects are relevant. First, the integrity of the control stack: decoder software, calibration data, pulse libraries, and the real-time pipeline that feeds syndrome data to the decoder all influence logical outcomes, so that tampering with a calibration file or with decoder weights could degrade or bias computations in a way that is hard to detect, since errors in a quantum computation are statistical. Measures that apply from conventional security engineering include signed and versioned configuration, authenticated access to control hardware, integrity-checked logs of calibration and decoding parameters, and separation of duties between those who operate and those who modify the system. In the risk assessment of Table III this threat has a modest occurrence score but a high severity and detection difficulty. Second, the strategic context: resource

estimates for breaking widely used public-key cryptosystems have fallen, with RSA-2048 factoring estimated first at about 20 million noisy qubits [30] and later at fewer than a million [31]. These estimates assume error rates and cycle times similar to those studied here. They do not mean that such machines exist, but they motivate the migration to post-quantum cryptographic standards, which NIST published in 2024 [32], particularly for data that must remain confidential for decades. Neither topic was evaluated experimentally in this paper.

Limitations

The study is a simulation with a simple noise model. All numbers depend on the assumed model, the choice of cycle time and idle exposure, and the matching decoder with known noise parameters, and none of the results are measurements of a physical device. The device profiles are illustrative. The extrapolations assume that the exponential suppression continues indefinitely. The threshold estimate has a finite-size drift. Decoder timing was measured in batch mode on one CPU, which does not represent the latency or the throughput of a deployed real-time system. The risk scores are expert judgements. Finally, the study considered a quantum memory only, and logical gates through lattice surgery, magic-state preparation, and the overheads of full algorithms add substantial cost beyond the memory overhead quantified here.

Conclusions

This paper studied fault-tolerant error correction in superconducting qubit arrays by circuit-level simulation of the rotated surface code. Under a standard uniform noise model, the suppression crossing lay at about 1.0% to 1.1%. Three device profiles showed that a combination of gate error 0.8%, readout error 3%, and T1 of 20 μs yielded no benefit from encoding, whereas a profile with 0.3% gate error, 0.8% readout error, and 70 μs coherence gave a suppression factor of 2.7, and a target profile with 0.2%, 0.5%, and 120 μs gave 4.3, reducing the projected overhead for a 10^{-9} per-round logical error from 2,449 to 1,057 physical qubits per logical qubit. Gate error was the dominant error source, accounting for about 90% of the logical error at distance 5 on the current profile, and a single-core software decoder reached the cycle time at distance 9, making real-time decoding a first-order constraint. The unmodelled mechanisms of leakage, crosstalk, and correlated bursts, together with the security of the classical control stack, define the agenda for further work. Future studies will incorporate leakage and correlated noise into the simulation, use non-uniform device models derived from measured calibration data, evaluate streaming and parallel decoders for latency, and extend the analysis from memory to logical operations.

REFERENCES

[1] Pawan Kumar Singh, Scaling Gate-All-Around (GAA) Transistor Architectures for Sub-2nm AI Accelerators Using Atomically Thin 2D Materials, Vol. 33 No. 08 (2024): JOCAAA, Journal Name: Journal of Computational Analysis and Applications, Journal's ISSN: 1521-1398 (Paper),1572-9206 (Online),

https://eudoxuspress.com/index.php/pub/article/view/5713
[2] Pawan Kumar Singh, Energy-Efficient Task Scheduling in Green Cloud Computing Using Neuromorphic Spiking Neural Networks, Vol. 33 No. 08 (2024): JOCAAA, Journal Name: Journal of Computational Analysis and Applications, Journal's ISSN: 1521-1398 (Paper),1572-9206 (Online), https://eudoxuspress.com/index.php/pub/article/view/5712
[3] Rangavinay Teja Royal Jagga, 2026, DOI: 10.1109/GCWCN66157.2025.11448495, Date of Conference: 22-23 November 2025, Date Added to IEEE Xplore: 25 March 2026 ,https://ieeexplore.ieee.org/document/11448495
[4] Rangavinay Teja Royal Jagga , 2026, Subtle Data Contamination in Visual AI: Covert Model Backdoors via Resampling Exploits, Date of Conference: 22-23 November 2025, Date Added to IEEE Xplore: 25 March 2026 ,https://ieeexplore.ieee.org/document/11448514
[5] Rangavinay Teja Royal Jagga, 2026, Robotic Tactile-Vision Integration for Interactive Object Disentanglement, https://ieeexplore.ieee.org/document/11448337
[6] Rangavinay Teja Royal Jagga, 2026, A Discounted Future Reward Framework for Intelligent Loyalty Optimization using CLTV-Aware Segmentation and Churn Prediction, https://ieeexplore.ieee.org/document/11497560
[7] Anjaneyulu Gudla; Manish Kumar; Vamshi Jeksani; Kiran Kumar Reddy; Gayathri Band, Harnessing Artificial Intelligence Cybersecurity: Cutting Edge Collaboration of SAP AWS to Safeguard Life Science Data. 2026 https://doi.org/10.1109/aiei69164.2026.11497833
[8] G. Mahender, Department of CSE(Data Science), Vardhaman College of Engineering ; Vamshi Jeksani; Manish Kumar; Koppuravuri Sri Lakshmi Sruthi; Kiran Kumar Reddy, SAP Cloud System on AWS for Risk Detection and Integration Artificial Intelligence Scalable Cybersecurity 2026 https://doi.org/10.1109/aiei69164.2026.11497435
[9] Kiran Kumar Reddy; Kamalakar Gunupati; Manish Kumar; Pell Reddy Rajender Reddy; Ramesh Julakanti; Ram Reddy Jonnalagadda, SAP System Optimization Using AI-Driven Process Automation and Predictive Modeling Maintenance for Enhanced Business Efficiency. 2025 https://doi.org/10.1109/computingcon64838.2025.11376613
[10] Amilineni, M.V. 2025. Audit-Safe Agentic RAG Framework for Regulated Enterprise Systems: A Trustworthy AI Architecture for SAP, Finance, Healthcare, and Government Workflows. INTERNATIONAL JOURNAL OF ADVANCES IN SIGNAL AND IMAGE SCIENCES. (Jan. 2025), 34–46. DOI: https://doi.org/10.29284/7fjzk883
[11] Pawan Kumar Singh, ACCELERATING LARGE LANGUAGE MODEL TRAINING USING HYBRID QUANTUM-CLASSICAL VARIATIONAL AUTOENCODERS WITH INTEGRATED PHOTONIC QRAM, Vol. 54 No. 3 (2026): July-September 2026, Power System Protection and Control, ISSN-1674-3415, https://pspac.info/index.php/dlbh/article/view/501, DOI: https://doi.org/10.46121/pspc.54.3.45
[12] Pawan Kumar Singh , RESILIENCE ASSESSMENT OF MODERN POWER GRID INFRASTRUCTURE AGAINST EXTREME WEATHER USING PHYSICS-INFORMED NEURAL NETWORKS, Vol. 54 No. 1 (2026): January-March 2026, Power System Protection and Control, ISSN-1674-3415,https://pspac.info/index.php/dlbh/article/view/502, DOI: https://doi.org/10.46121/pspc.54.1.64
[13] Pawan Kumar Singh, MITIGATING THE EXABYTE STORAGE CRISIS: ENHANCING READ/WRITE EFFICIENCY IN 5D OPTICAL GLASS STORAGE USING SILVER NANOPARTICLE DOPING, Vol. 38 No. 11s (2025), International Journal of Applied Mathematics (IJAM) , pISSN

1311-1728, eISSN 1314-8060 ,https://ijamjournal.org/ijam/publication/index.php/ijam/article/view/2153

[14] Mr. Pawan Kumar Singh (Author), Miss. Pari Nidhi Singh (Author) ,Intelligent Bot, ASIN : B0DBGCQY8X,Publisher : Namya Press, Publication date : November 25, 2022,Language : English, Print length : 105 pages,ISBN-10 : 9390124867,ISBN-13 : 978-9390124862,Item Weight : 7.5 ounces, Dimensions : 6.24 x 0.43 x 9.24 inches,https://www.amazon.com/Intelligent-Bot-Pawan-Kumar-Singh/dp/B0DBGCQY8X/ref=sr_1_5?crid=2VAXN5BRN5SMS&dib=eyJ2IjoiMSJ9.v3OCQvHBpy20RIjfMWh0qbOl-RLOlUJIC8Xa0Pjeqilvo2sbZ_suN3LbSCw_OA_ZD_4lgjRLMGlBwZQQ1ehZEfDpt_MJiOUfVuqqzMav0I5_mb6pN5DQog0U7SA826n1DQQ3QAtWwopHy4lC5IfhZXttKj9faiyATwhdtDATSSV1-r7FmzM2VQyIA0jxcfq6E6hp9ECfH1fby0li9kUfGpLxMq4GktlzUIJO5ggrhsQ.G1AjQiVqU4HFsnSczvz-X6NXCNs3EFSn-RI8mcWWGOc&dib_tag=se&keywords=Pawan+Kumar+Singh%2C+book&qid=1787815741&sprefix=pawan+kumar+singh%2C+bo%2Caps%2C450&sr=8-5

[15] Mr. Pawan Kumar Singh (Author), STORAGE CRISES DUE TO RISE OF AI: A Comprehensive Guide to Managing the Storage Challenges in the Age of Artificial Intelligence, ASIN : B0HFK12ZCT
Publisher : EB1 Profile, Accessibility : Learn more, Publication date : August 17, 2026,Edition : 1st
Language : English, File size : 1.7 MB, Screen Reader : Supported, Enhanced typesetting : Enabled
X-Ray : Not Enabled, Word Wise : Not Enabled ,Print length : 261 pages ,ISBN-13 : 979-8951479112,Page Flip : Enabled, https://www.amazon.com/STORAGE-CRISES-DUE-RISE-Comprehensive-ebook/dp/B0HFK12ZCT/ref=sr_1_1?crid=9MF6C4WDVJR5&dib=eyJ2IjoiMSJ9.DQ8fesBch7ELmRnilDt-YA.NBSCHLmetvnbhkxwIpOoj3s0IVsCV8y6-ZCfCP6Ul1c&dib_tag=se&keywords=Pawan+Kumar+Singh%2C+book%2C+eb1+Profile&qid=1787816040&sprefix=pawan+kumar+singh%2C+book%2C+eb1+profile%2Caps%2C420&sr=8-1

[16] Parag Bharatkumar Parikh, FRAMEWORKS FOR MITIGATING SUPPLY CHAIN DISRUPTIONS AND MATERIAL PRICE VOLATILITY IN SUSTAINABLE BUILDING CONSTRUCTION, Vol. 53 No. 2 (2025): April-June 2025 , , Power System Protection and Control, ISSN-1674-3415, https://pspac.info/index.php/dlbh/article/view/447, DOI: https://doi.org/10.46121/pspc.53.2.34

[17] Parag Bharatkumar Parikh, IMPLEMENTING DIGITAL INSPECTION PROTOCOLS FOR ENHANCED QUALITY CONTROL MANAGEMENT IN HIGH-RISE CONSTRUCTION, Vol. 54 No. 3 (2026): July-September 2026, Power System Protection and Control, ISSN-1674-3415, https://pspac.info/index.php/dlbh/article/view/439, DOI: https://doi.org/10.46121/pspc.54.3.12

[18] Parag Bharatkumar Parikh , EVALUATING THE FEASIBILITY AND EFFICIENCY OF 3D-PRINTED CONCRETE TECHNOLOGY IN SUSTAINABLE MODULAR CONSTRUCTION, Power System Protection and Control, ISSN-1674-3415, https://pspac.info/index.php/dlbh/issue/view/30, DOI: https://doi.org/10.46121/pspc.54.1.61

[19] Parag Bharatkumar Parikh, EVALUATING THE FEASIBILITY AND EFFICIENCY OF 3D-PRINTED CONCRETE TECHNOLOGY IN SUSTAINABLE MODULAR CONSTRUCTION, Vol. 54 No. 1 (2026): January-March 2026, System Protection and Control, ISSN-1674-3415, https://pspac.info/index.php/dlbh/article/view/440, DOI:

https://doi.org/10.46121/pspc.54.1.61
[20] Ronakkumar shah, REDEFINING BUSINESS PROCESS MANAGEMENT: THE SYNERGY OF AI AND INTELLIGENT AUTOMATION, Vol. 54 No. 3 (2026): July-September 2026, System Protection and Control, ISSN-1674-3415, https://pspac.info/index.php/dlbh/article/view/448, DOI: https://doi.org/10.46121/pspc.54.3.14
[21] Ronakkumar shah, OPERATIONAL ACCOUNTABILITY IN ACTION: METRICS AND MECHANISMS FOR SYSTEMIC SUCCESS, Vol. 53 No. 4 (2025): October-December 2025, System Protection and Control, ISSN-1674-3415, https://pspac.info/index.php/dlbh/article/view/452, DOI: https://doi.org/10.46121/pspc.53.4.40
[22] Ronakkumar shah, BEYOND THE BLUEPRINT: AUTOMATED WORKFLOW ENFORCEMENT AND POLICY GOVERNANCE, Vol. 53 No. 2 (2025): April-June 2025 , System Protection and Control, ISSN-1674-3415 ,https://pspac.info/index.php/dlbh/article/view/451, DOI: https://doi.org/10.46121/pspc.53.2.35
[23] Tushita Agarwal; Swaminathan Sethuraman, Mapping Customer Behavior: Visual Analysis of Online Retail Interactions, Date Added to IEEE Xplore: 17 February 2026, DOI: https://doi.org/10.1109/IC2NC67409.2025.11376261
[24] Tushita Agarwal, Efficient Data Summarization and Comparison via Grid-Based Statistical Proxies for Large-Scale Datasets, Date Added to IEEE Xplore: 03 December 2025, DOI: https://doi.org/10.1109/ICBATS66542.2025.11258564
[25] Dip Bharatbhai Patel, Building scalable business intelligence systems in the cloud: A technical approach, International Journal of Science and Research Archive, 2021, 02(01), 212-215., Received on 03 February 2021; revised on 17 April 2021; accepted on 19 April 2021,DOI: https://doi.org/10.30574/ijsra.2021.2.1.0047
[26] Dip Bharatbhai Patel, University of North America, Virginia, USA, Home / Archives / Vol. 5 No. 02 (2025): Volume 05 Issue 02 / Articles, https://www.academicpublishers.org/journals/index.php/ijdsml/article/view/5958
[27] Sai Akshara Vemuri , KINEMATIC OPTIMISATION OF SOFT ROBOTIC MANIPULATORS FOR MEDICAL INTERVENTION, Vol. 54 No. 3 (2026): July-September 2026, System Protection and Control, ISSN-1674-3415, https://pspac.info/index.php/dlbh/article/view/450
[28] Sai Akshara Vemuri, https://www.periodicos.ulbra.org/index.php/acta/article/view/528
[29] Aziz, A., Chandusha, K., Naga Kiran, B., Prasad, M. L. M., Golla, K., Rajeswari, S., & Katta, S. K. R. (2026). Exploring Machine Learning Applications for Genomic Data Analysis in Personalized Medicine. International Journal of Drug Delivery Technology, 16(38s), 1166-1173. https://doi.org/10.25258/ijddt.16.38s.127,https://www.periodicos.ulbra.org/index.php/acta/article/view/687
[30] Mohammad Naffizuddin , Chaganti Ashok ,Sowjanya Gunukula , Rvbs Sarma , Bhavana Sujanamulk , Bharani Krishna Takkella , Chukka Ram Sunil ,Varri Sujana , Ashwini Kumar, Etiological Factors of Orofacial Clefts in a Hospital-Based Population: A Descriptive Analytical Study, Published: December 10, 2025,DOI: 10.7759/cureus.98868,DOI : https://doi.org/10.7759/cureus.98868
[31] Manoj Kumar Kagitha, Automated Security Compliance in Ci/Cd: A Natural Language Processing (NLP) Approach to Detecting Vulnerabilities in Infrastructure-As-Code (Terraform/Bicep), Publication year 2021, Volume 2021, Issue 12, https://computerfraudsecurity.com/index.php/journal/article/view/970
[32] Manoj Kumar Kagitha, Hybrid Quantum-Classical Resource Scheduling: A Proposed Architecture for Next-Generation Hyperscale Data Centers,

Publication year 2024, Volume 2024, Issue 12, https://computerfraudsecurity.com/index.php/journal/article/view/969

[33] Manoj Kumar Kagitha, Self-Healing Cloud Infrastructure: A Hybrid Reinforcement Learning Framework for Predicting Microservice Failures in Azure Kubernetes Service (AKS),Publication year 2023, Volume 2023, Issue 12,https://computerfraudsecurity.com/index.php/journal/article/view/971

[34] Manoj Kumar Kagitha, GREENOPS IN THE CLOUD: AN AI-DRIVEN TELEMETRY ANALYSIS MODEL FOR REDUCING CARBON FOOTPRINT IN HIGH-AVAILABILITY CLUSTERS, Vol. 28 No. 6 (2020): JOCAAA, https://www.eudoxuspress.com/index.php/pub/article/view/5054

[35] Lakshmi Rahul Reddy Mareddy. (2026). Security and Performance Assessment of Encryption Techniques for Cloud Platforms. International Journal of Communication Networks and Information Security (IJCNIS), 18(1), 68–80. Retrieved from https://ijcnis.org/index.php/ijcnis/article/view/8735

[36] Lakshmi RahulReddy Mareddy, Context-Aware Learning Approaches for Improving Prediction Accuracy in Dynamic Systems, International Journal of Computational Mathematical Ideas (IJCMI), Vol.17 No.3(2025): IJCMI Vol17 NO3 2025 https://www.ijcmi.com/index.php/journal/article/view/15

[37] Lakshmi Rahul Reddy , Mareddy. (2026). Revisiting Autonomy in Artificial Intelligence through Agentic System Design. Journal of Computational Analysis and Applications (JoCAAA), 35(1), 707–713. https://eudoxuspress.com/index.php/pub/article/view/4780

[38] Mahendrakumar Kalal, Lean-Driven SAP Production Planning Optimization Using Machine Learning for Inventory and Throughput Efficiency, Date of Conference: 19-20 March 2026, Date Added to IEEE Xplore: 08 April 2026,ISBN Information:,ISSN Information: DOI:10.1109/ISDFS69419.2026.11459029, https://ieeexplore.ieee.org/abstract/document/11459029

[39] Mahendra kumar Kalal, SUPPLY CHAIN RESILIENCE THROUGH INTEGRATED SAP PRODUCTION PLANNING – PROCUREMENT SYNCHRONIZATION, Archives / Vol. 54 No. 1 (2026): January-March 2026 / Articles, https://pspac.info/index.php/dlbh/article/view/259

[40] Dr Manoj Goel (December 2018). THE ATTITUDE OF DIFFERENT STATES STUDENTS TOWARDS PHYSICAL EDUCATION; STUDYING IN PHYSICAL EDUCATION COLLEGES OF MAHARSHTRA STATE, https://ijeponline.com/index.php/journal/article/view/965/847

[41] Ilakiya Ulaganathan, Tagore Engg. College, Anna University, Chennai, India, ; FNU Antara; Santhosh Chitraju Gopal Varma; Zokir Mamadiyarov; Ziyadulla Turayev, Published in: 2025 International Conference on Sustainability, Innovation & Technology (ICSIT), Date of Conference: 22-23 August 2025, Date Added to IEEE Xplore: 19 December 2025, ISBN Information: https://ieeexplore.ieee.org/document/11294748/references#references

[42] Shreyas Kasture, Sudhanshu Maurya, Amit Kumar Sharma, Santhosh Chitraju Gopal Varma, Kashish Mirza, Firdous Sadaf Mohammad Ismail, DOI: http://doi.org/10.11591/ijai.v15.i2.pp1746-1761, IAES International Journal of Artificial Intelligence (IJ-AI), ISSN/e-ISSN 2089-4872/2252-8938 https://ijai.iaescore.com/index.php/IJAI/article/view/26932

[43] Shiv Shankar Dwivedi, Mr. Santosh Kumar Sharma, Future-Proofing Data Security with Quantum-Resistant Cryptography, Vol. 11 No. 3 (2025): IJCESEN, DOI: https://doi.org/10.22399/ijcesen.3447, https://ijcesen.com/index.php/ijcesen/article/view/3447

[44] Vijender Kalmotia, Enhancing statistical accuracy in gene perturbation studies, Volume 266, August 2026, 105819, https://doi.org/10.1016/j.biosystems.2026.105819, https://www.sciencedirect.com/science/article/pii/S0303264726001292

[45] Naveen Undrathi, Design and implementation of generative AI-driven data transformation pipelines using spring boot for scalable financial applications, eISSN: 2581-9615 || CODEN: WJARAI || Impact Factor 8.2 || CrossRef DOI, September 2026 (Volume 31, Issue 3), DOI url: https://doi.org/10.30574/wjarr.2026.30.3.1629,
[46] Naveen Undrathi, Agentic generative AI-enabled microservices framework for intelligent financial data processing in java-based enterprise systems, September 2026 (Volume 31, Issue 3), eISSN: 2581-9615 || CODEN: WJARAI || Impact Factor 8.2 || https://doi.org/10.30574/wjarr.2026.30.3.1628
[47] Akshay Jain, Comparative Analysis of Linkage Methods in Hierarchical Clustering for Customer Segmentation, Conference paper, First Online: 07 October 2025, https://link.springer.com/chapter/10.1007/978-981-96-7289-9_44

[48] Ismail Hossain, Department of Computer Science, George Mason University, Fairfax, VA, USA, Mridul Banik, Department of Computer Science, Colorado State University, Fort Collins, CO, USA, https://ieeexplore.ieee.org/abstract/document/11446534 ,,DOI: 10.1109/FMLDS67896.2025.00106
[49] Ismail Hossain, Mridul Banik , Fahmid Al Farid , Jia Uddin , Hezerul bin Abdul Karim , Advancing Large Language Models for Low-Resource Languages: A Systematic Review of Pretraining, Adaptation, and Ethical Challenges, 10.32604/cmes.2026.075507, Date: 2026
https://www.sciencedirect.com/org/science/article/pii/S152614922600322X
[50] Ismail Hossain; Mridul Banik, Bridging Visual and Linguistic Intelligence for Chest X-rays: A Comprehensive Review of ViTs and LLM Synergies, Published in: 2025 IEEE International Conference on Future Machine Learning and Data Science (FMLDS) Date of Conference: 02-05 November 2025, Date Added to IEEE Xplore: 25 March 2026, ISBN Information: https://ieeexplore.ieee.org/abstract/document/11446534
[51] Rifat Sarker Aoyon1, Ismail Hossain2, M. Abdullah-Al-Wadud3, Jia Uddin4, A Secured and Continuously Developing Methodology for Breast Cancer Image Segmentation via U-Net Based Architecture and Distributed Data Training, https://www.sciopen.com/article/10.32604/cmes.2025.060917
[52] M. B. Vibha, M. Chandrika, Samitha Khaiyum & P. Rakshitha Kiran, Predicting sedentary behavior in adults using stacked LSTM modeling, published: 27 November 2024
Volume 16, pages 346–355 (2025), https://link.springer.com/article/10.1007/s13198-024-02622-2
[53] Bellary Chiterki Anil, Jayasimha Sondekoppa Rajkumar, T. L. Divya, Samitha khaiyum
Rakshitha Kiran P., Balakrishnan Ramadoss, A Radiomics-based Framework for Liver Cancer Analysis using Explainable Artificial Intelligence (XAI) Methods, Vol. 15 No. 3 (2025): June, 2025, https://etasr.com/index.php/ETASR/article/view/10377
[54] Jayminkumar Patel, Sanjaykumar patel, Birju Patel, Rajan shah, Development and Validation of a Stability-Indicating Analytical Method for Quantitative Determination of Selected Anticancer Drugs in Pharmaceutical Dosage Form, Archives / Vol. 35 No. S2 (2026): Apr-jun 2026, https://welltestingjournal.com/index.php/WT/article/view/288
[55] Jayminkumar Patel, Sanjaykumar patel, Birju Patel, Rajan shah, Artificial Intelligence-Guided Optimization of Chromatographic Methods for Pharmaceutical Analytical Development, Archives / Vol. 35 No. S2 (2026): Apr-jun 2026, https://welltestingjournal.com/index.php/WT/article/view/294

[56] Sharoon Sharif, Inikpi Egbunu, Yujian Fu, and Zhigang Xiao. 2026. Hybrid Multi-Modal Learning for Extreme Long-Tail Fungi Classification. In 2026 ACM Southeast Conference (ACMSE 2026), April 23–25, 2026, Troy, AL, USA. ACM, New York, NY, USA, 38–45. https://doi.org/10.1145/3746467.3801502

[57] A. Chandrakumaran, "Innovative Strategies for Real-Time Analytics in Modern Data Warehousing Using Dockerized Ecosystems," 2025 International Conference on Advances in Next-Gen Computer Science (ICANCS), Bangalore, India, 2025, pp. 1-6, doi: https://doi.org/10.1109/ICANCS65819.2025.11377462

[58] A. Chandrakumaran, "Enhancing SAP Predictive Maintenance and Industrial Analytics with LLM-Driven Automation," 2025 IEEE Madhya Pradesh Section Conference (MPCON), Jabalpur, India, 2025, pp. 238-244, doi: https://doi.org/10.1109/MPCON66082.2025.11256577.

[59] A. Chandrakumaran, "Enhancing SAP Cloud Optimization with Explainable AI: Cost Control, Workload Forecasting, and Performance Enhancement," 2025 3rd International Conference on Inventive Computing and Informatics (ICICI), Bangalore, India, 2025, pp. 456-463, doi: https://doi.org/10.1109/ICICI65870.2025.11069968.

[60] A. Chandrakumaran, "Innovative Strategies for Real-Time Analytics in Modern Data Warehousing Using Dockerized Ecosystems," 2025 International Conference on Advances in Next-Gen Computer Science (ICANCS), Bangalore, India, 2025, pp. 1-6, doi: https://doi.org/10.1109/ICANCS65819.2025.11377462.

[61] Ashwini Chandrakumara, year :2025, Leveraging Autonomous AI for Agile Growth: Transforming Project Management in Fast-Scaling Startups, Proceedings of the 2nd International Conference on Sustainable Business Practices and Innovative Models (ICSBPIM-2025), pages :730-743, issn :2352-5428, isbn :978-94-6463-872-1, Atlantis Press https://doi.org/10.2991/978-94-6463-872-1_46

[62] Anasuya Patil 1, Gurinderdeep Singh 2, Rajendra Dnyandeo Dighe 3, Dhruv Dev 4, Bhaveshkumar A Patel 5, Samatha Rudrangi 6, Gaurav Tiwari 7, Preparation, optimization, and evaluation of ligand-tethered atovaquone-proguanil-loaded nanoparticles for malaria treatment, 2025 Apr;36(6):711-742. doi: 10.1080/09205063.2024.2422704. Epub 2024 Nov 10., https://pubmed.ncbi.nlm.nih.gov/39522102/

[63] Kancharla Vijayalakshmi, Bethapudi Samuel Anand Andrews, Estimation of Cyproheptadine Hydrochloride and Tricholine Citrate Simultaneously in Syrup Dose by Applying Stability Indicating HPLC Methodology, December 31, 2020, Vol. 11, Issue 4, Pages 1813–1819, DOI: 10.26452/ijrps.v11iSPL4.4383, https://ijrps.com/v11si4/3683

[64] Vijayalakshmi Kancharla ,Kumar Abbaraju V D N, Andrews B S A, Nagaraju Dasari, Nagu Korupolu, Melphan as Anticancer and New Insights of Drug as Parenteral Dosage form against SARS-CoV-2 by Using Development and Validation , November 18, 2020, Vol. 11, Issue 1, Pages 1437–1446 DOI: 10.26452/ijrps.v11iSPL1.3686, https://ijrps.com/v11si1/2911

[65] Ramesh, D., A. Singh, and L. H. Channaiah. 2026. " Evaluating the Effectiveness of Chewy Chocolate Chip Granola Bar Manufacturing Process on Salmonella Survival." Food Science & Nutrition 14, no. 4: e71698. https://doi.org/10.1002/fsn3.71698.

[66] Inventor: Akhilesh RaiDilip Srinivas Krovi Sarthak Saptarshi Bandopadhyay Ravinder Singh Choudhary Richard LAWTON, 2025-02-28, Priority to US19/067,141,2025-11-14,Assigned to CITIBANK, N.A.,2025-12-30,Application granted,2025-12-30, Publication of US12511187B, https://patents.google.com/patent/US12511187B1/en?oq=US12511187

[67] Vivekanandan Govindan Ekambaram , REAL-TIME AUTOMATED DEFECT DETECTION IN INDUSTRIAL MANUFACTURING USING DEEP LEARNING AND TEXTURE ANALYSIS, Archives ,Vol. 54 No. 4 (2026): October-December 2026, Power System Protection and Control, ISSN-1674-3415,DOI: https://doi.org/10.46121/pspc.54.4.06, https://pspac.info/index.php/dlbh/article/view/545
[68] Vivekanandan Govindan Ekambaram, Yamuna Natarajan, AN OPTIMIZED HYBRID FRAMEWORK FOR REAL-TIME EDGE DETECTION AND FEATURE EXTRACTION IN AUTONOMOUS VEHICLE VISION SYSTEMS, Vol. 54 No. 4 (2026): October-December 2026 , Power System Protection and Control, ISSN-1674-3415, DOI: https://doi.org/10.46121/pspc.54.4.05, https://pspac.info/index.php/dlbh/article/view/544
[69] John Smart Mgbakor, Behavioral Health Equity In High-Disparity Urban Communities: Public Health Impact, National Scalability, And Clinical Practice Implications, Pages1166 – 1177Cover Date, August 2026, Volume34, Issue, Special Issue 7- Fundamental Studies, Print ISSN-0965-7452, Electronic- ISSN-2396-8893, DOI: 10.1922/ejprd.v34i7s.1767, https://www.ejprd.org/article.php?article_id=1767&journal_id=171
[70] Nikhil Kumar Singh, Binay K. Singh, Piyush Kumar, Avinash Pandey, Sudhir Kumar, Sujit Kumar Bishi, A. Pattanayak, V. P. Bhadana, Sujay Rakshit & Kishor U. Tribhuvan, Integrative genomic and machine learning approaches reveal evolutionary signatures in the winged bean mitochondrial genome, Published: 28 November 2025,Volume 26, article number 3 (2026), https://link.springer.com/article/10.1186/s12870-025-07738-6
[71] GAURAV KUMAR SINHA, Year 2026 https://mathsapplication.com/article-view/?id=223
[72] GAURAV KUMAR SINHA, Year 2026 , https://mathsapplication.com/article-view/?id=224
[73] GAURAV KUMAR SINHA, Year 2026 , https://mathsapplication.com/article-view/?id=225
[74] Rasmi Ranjan Choudhury, Design and Implementation of a Tuned Rear Axle Bending Damper for Beat Boom Noise Mitigation in SUV Driveline Systems, 2026 International Conference, https://ieeexplore.ieee.org/document/11746870/authors#authors
[75] Rasmi Ranjan Choudhury, Comparative Performance Analysis of Single-Speed Versus Multi-Speed Transmissions in Battery Electric, 2026 International Conference, https://ieeexplore.ieee.org/document/11746704
[76] Nithesh Gudipuri1, Lalith Chandra Bandaru2, Mohammed Shakeer Bandrevu, SCALABLE DATA ENGINEERING FRAMEWORKS FOR REAL-TIME PROCESSING IN DISTRIBUTED SYSTEMS, Published:2026-10-18,Pages:444-453, https://actainnovations.com/index.php/pub/article/view/1900 ,doi: 10.62441/actainnovations.vi.1900
[77] Mohammed Shakeer Bandrevu; Pratham Patkar; Janardhana Naidu Kola, Trustworthy AI Models for Secure Data Processing Environments, Published in: 2026 International Conference on Natural Language Processing and Computer Vision (ICNPCV),Date of Conference: 17-18 July 2026, DOI: 10.1109/ICNPCV69434.2026.11708997, https://ieeexplore.ieee.org/document/11708997/authors#authors,
[78] Lalith Chandra Bandaru; Venkateswara Rao Batta; Uday Kumar Reddy Gangula, Hybrid AI and Data Analytics Frameworks for Cyber Resilience, 2026 International Conference on Natural Language Processing and Computer Vision (ICNPCV),Date of Conference: 17-18 July 2026,DOI: 10.1109/ICNPCV69434.2026.11708795, https://ieeexplore.ieee.org/document/11708795

[79] Lalith Chandra Bandaru; Karimulla Syed,Head of Access Management, S&P Global, Raleigh, NC, USA
[80] ; Nishanth Vepachedu; Rajmani Singh Oinam; Raja Vignesh Vaithiyalingam; Quazi Taif Sadat, Advanced Secure Knowledge Extraction Techniques for Large Language Models, 2026 International Conference on Emerging in Computing Technologies (INCECT),Date of Conference: 21-22 August 2026, DOI: 10.1109/INCECT72370.2026.11742788, https://ieeexplore.ieee.org/document/11742788
[81] Mohammed Shakeer Bandrevu, Independent Researcher, Aubrey, TX, USA, ; NagaSatyanarayana Raju Uppalapati; Ramesh Bellamkonda; Srikanth Kamatala, Llm-Augmented Cyber Threat Detection Using Federated Edge Intelligence and Data Mining Techniques, Published in: 2025 International Conference on Computing Technologies & Data Communication (ICCTDC),Date of Conference: 04-05 July 2025, https://ieeexplore.ieee.org/document/11158153 , DOI: 10.1109/ICCTDC64446.2025.11158153
[82] Ankit Pathak, Leveraging AI for Better Data Quality and Insights, Volume 7 Issue 3 (2025), https://doi.org/10.32996/jcsts.2025.7.2.19, https://al-kindipublisher.com/index.php/jcsts/article/view/9345
[83] Uma Rajeswari Batchu, Bharati Reddi, Joshna Rani Surapaneni, Aruna Jangam, Sunil Misra, Anthony Addlagatta & Prakasham Reddy Shetty, Inhibition of Xanthine Oxidase by 1-O-Methyl Chrysophanol, A Hydroxyanthraquinone Isolated from Amycolatopsis Thermoflava ICTA 103, Published: 13 December 2025,Volume 66, pages 1049–1068 (2026) https://link.springer.com/article/10.1007/s12088-025-01534-4
[84] GAURAV KUMAR SINHA, Year 2025, https://visualcompublications.es/SAUC/article/view/6525
[85] GAURAV KUMAR SINHA, Year 2025, https://visualcompublications.es/SAUC/article/view/6526
[86] GAURAV KUMAR SINHA, Year 2025, https://visualcompublications.es/SAUC/article/view/6527

[87] D Benito Johnson 1, Gurinderdeep Singh 2, Deeksha Sharma 3, Venkatesan Natarajan 4, Knv Chenchu Lakshmi 5, Ram C Dhakar 6, Sadhana R Shahi 7, Suresh Velayutham 8, Ruchi Tiwari 9, Exploring Computational Advancements in ADME: Essential Insights for Drug Disposition, PMID: 39496312 DOI: 10.62958/j.cjap.2024.033, https://pubmed.ncbi.nlm.nih.gov/39496312/
[88] Mohammed Shakeer Bandrevu, Service Now Ebonding Methods, Implementation and Key features Published,30 Nov 2024, https://ijcttjournal.org/archives/ijctt-v72i11p125